MCP1415/16

Tiny 1.5A, High-Speed Power MOSFET Driver

Features

- High Peak Output Current: 1.5A (typical)
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
  - 470 pF in 13 ns (typical)
  - 1000 pF in 18 ns (typical)
- Short Delay Times: 44 ns (t_{D1}), 47 ns (MCP1415 t_{D2}), 54 ns (MCP1416 t_{D2}) (typical)
- Low Supply Current:
  - With Logic '1' Input - 0.65 mA (typical)
  - With Logic '0' Input - 0.1 mA (typical)
- Latch-Up Protected: Withstands 500 mA Reverse Current
- Logic Input Withstands Negative Swing up to 5V
- Space-Saving 5L SOT-23 Package

Applications

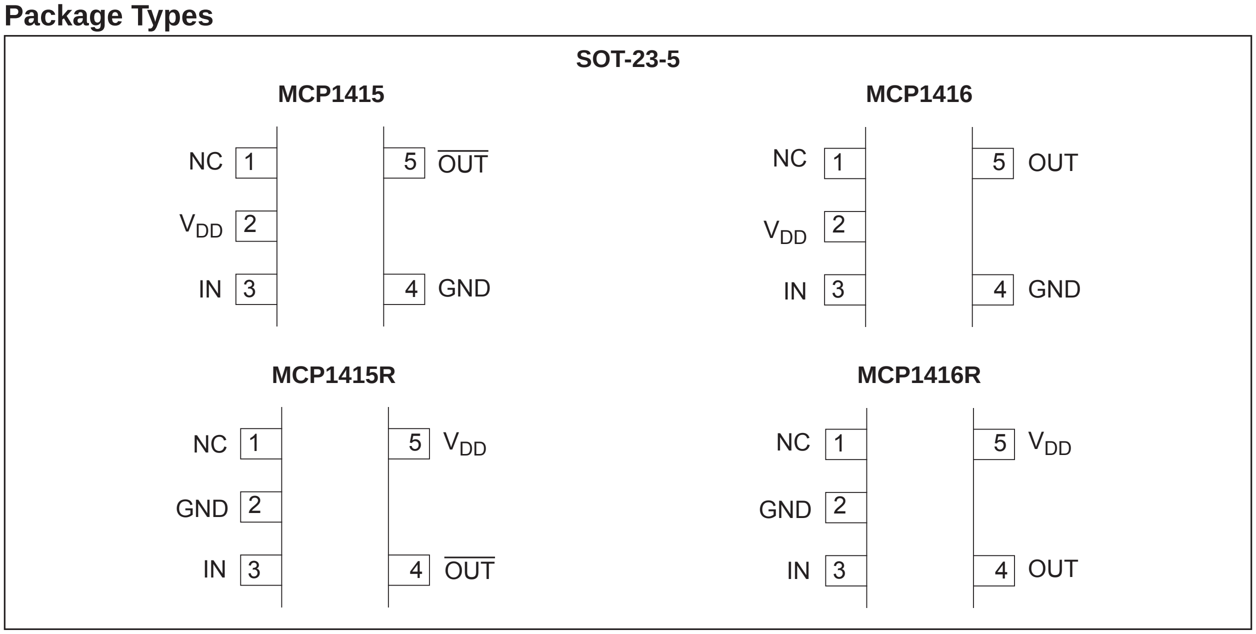
- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Level Translator
- Motor and Solenoid Drive

General Description

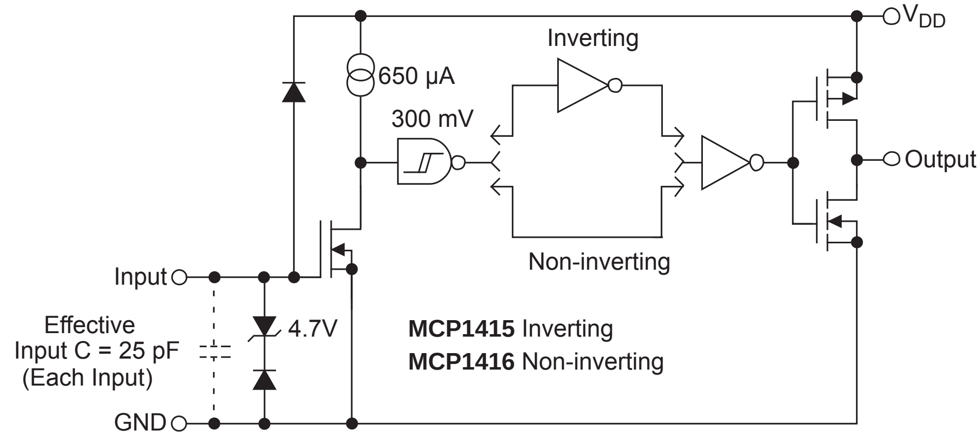
The MCP1415/16 devices are high-speed, dual MOSFET drivers that are capable of providing up to 1.5A of peak current while operating from a single 4.5V to 18V supply. The inverting or non-inverting single channel output is directly controlled from either TTL or CMOS (3V to 18V) logic. These devices also feature low shoot-through current, matched rise and fall time, and short propagation delays which make them ideal for high switching frequency applications. They provide low enough impedances in both the 'On' and 'Off' states to ensure the intended state of the MOSFET is not affected, even by large transients.

These devices are highly latch-up resistant under any condition within their power and voltage ratings. They are not subject to damage when noise spiking (up to 5V, of either polarity) occurs on the Ground pin. They can accept up to 500 mA of reverse current being forced back into their outputs without damage or logic upset. All terminals are fully protected against electrostatic discharge (ESD) up to 2.0 kV (HBM) and 300V (MM).

Package Types



Functional Block Diagram



Note: Unused inputs should be grounded.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}, Supply Voltage .... +20V
V_{IN}, Input Voltage .... (V_{DD} + 0.3V) to (GND - 5V)
Package Power Dissipation (T_A = 50°C)
5L SOT23 .... 0.39W
ESD Protection on all Pins .... 2.0 kV (HBM)
.... 300V (MM)

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic ‘1’ High Input Voltage	V_{IH}	2.4	1.9	—	V	
Logic ‘0’ Low Input Voltage	V_{IL}	—	1.6	0.8	V	
Input Current	I_{IN}	-1	—	+1	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	-5	—	V_{DD} + 0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} - 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	6	7.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V (**Note 1**)
Output Resistance, Low	R_{OL}	—	4	5.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V (**Note 1**)
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V (**Note 1**)
Latch-Up Protection Withstand Reverse Current	I_{REV}	0.5	—	—	A	Duty cycle ≤ 2%, t ≤ 300 µs (**Note 1**)
Switching Time (Note 1)						
Rise Time	t_R	—	18	25	ns	V_{DD} = 18V, C_L = 1000 pF Figure 4-1, Figure 4-2 (**Note 1**)
Fall Time	t_F	—	21	28	ns	V_{DD} = 18V, C_L = 1000 pF Figure 4-1, Figure 4-2 (**Note 1**)
Delay Time	t_{D1}	—	44	54	ns	V_{DD} = 18V, V_{IN} = 5V Figure 4-1, Figure 4-2 (**Note 1**)
MCP1415 Delay Time	t_{D2}	—	47	57	ns	V_{DD} = 18V, V_{IN} = 5V Figure 4-1 (**Note 1**)
MCP1416 Delay Time	t_{D2}	—	54	64	ns	V_{DD} = 18V, V_{IN} = 5V Figure 4-2 (**Note 1**)
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_S	—	0.65	1.1	mA	V_{IN} = 3V
	I_S	—	0.1	0.15	mA	V_{IN} = 0V

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE) (Note 1)

Electrical Specifications: Unless otherwise indicated, over the operating range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	-5	—	V_{DD} + 0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} - 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	8.5	9.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	6	7	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time						
Rise Time	t_R	—	26	37	ns	V_{DD} = 18V, C_L = 1000 pF Figure 4-1, Figure 4-2
Fall Time	t_F	—	29	40	ns	V_{DD} = 18V, C_L = 1000 pF Figure 4-1, Figure 4-2
Delay Time	t_{D1}	—	60	70	ns	V_{DD} = 18V, V_{IN} = 5V Figure 4-1, Figure 4-2
MCP1415 Delay Time	t_{D2}	—	62	72	ns	V_{DD} = 18V, V_{IN} = 5V Figure 4-1
MCP1416 Delay Time	t_{D2}	—	72	82	ns	V_{DD} = 18V, V_{IN} = 5V Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_S	—	0.75	1.5	mA	V_{IN} = 3.0V
	I_S	—	0.15	0.25	mA	V_{IN} = 0V

Note 1: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 5LD SOT23	θ_{JA}	—	220.7	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ = 18V.

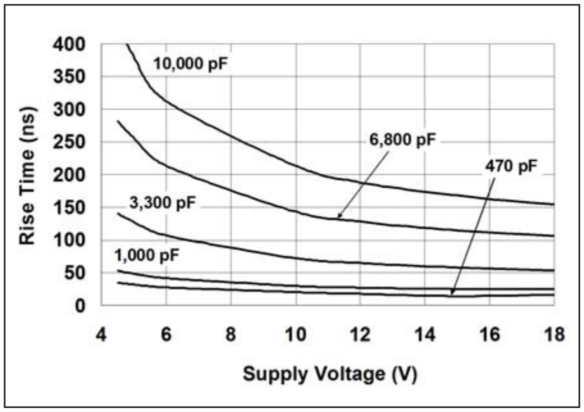


FIGURE 2-1: Rise Time vs. Supply Voltage.

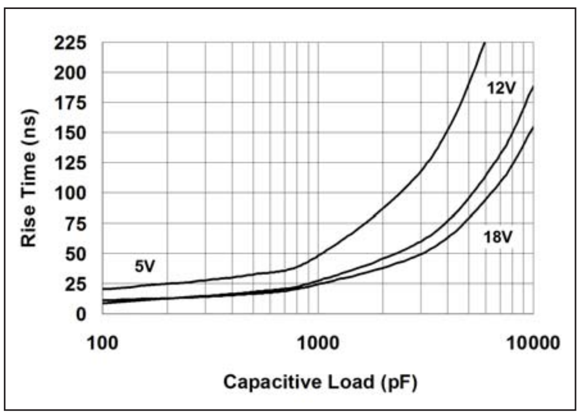


FIGURE 2-2: Rise Time vs. Capacitive Load.

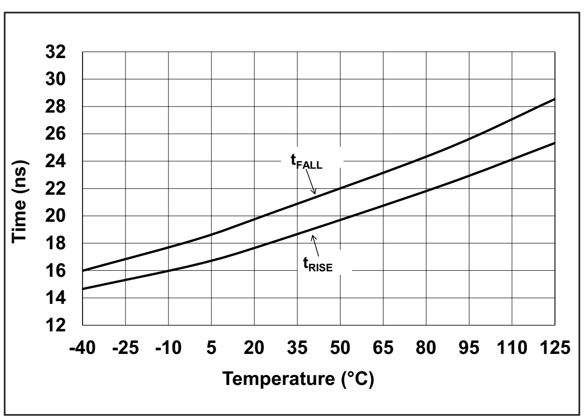


FIGURE 2-3: Rise and Fall Times vs. Temperature.

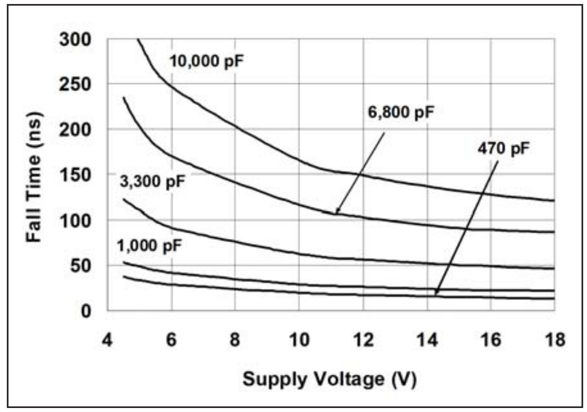


FIGURE 2-4: Fall Time vs. Supply Voltage.

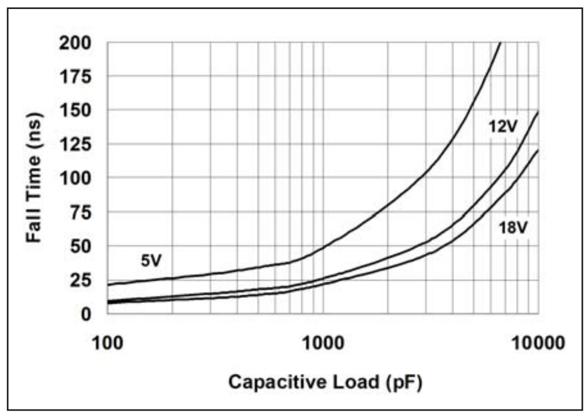


FIGURE 2-5: Fall Time vs. Capacitive Load.

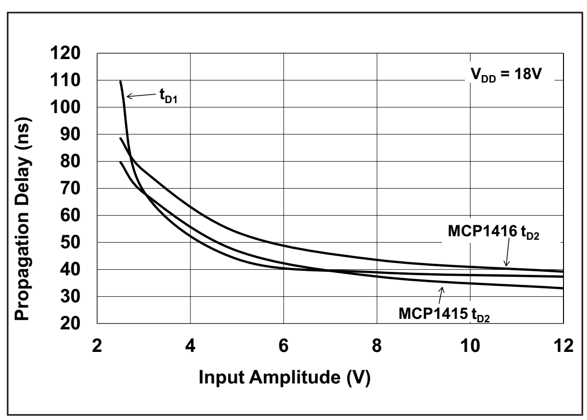


FIGURE 2-6: Propagation Delay Time vs. Input Amplitude.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ = 18V.

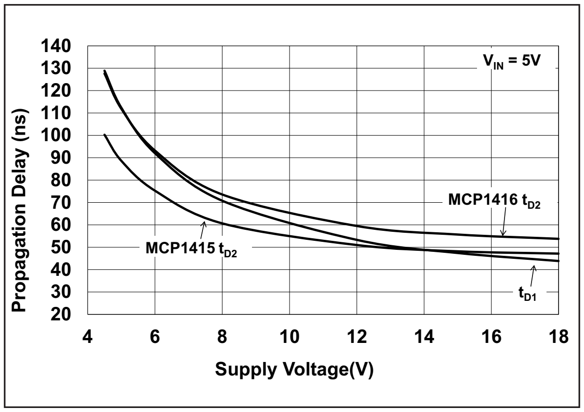


FIGURE 2-7: *Propagation Delay Time vs. Supply Voltage.*

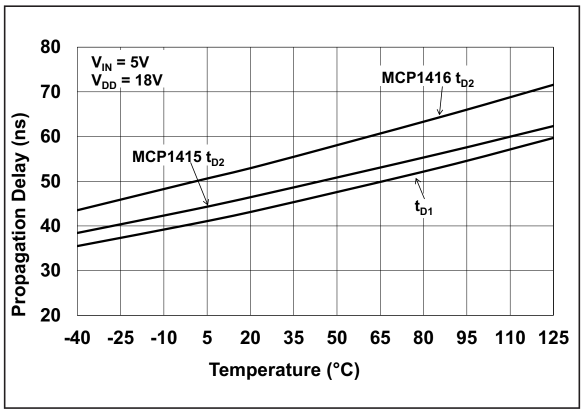


FIGURE 2-8: *Propagation Delay Time vs. Temperature.*

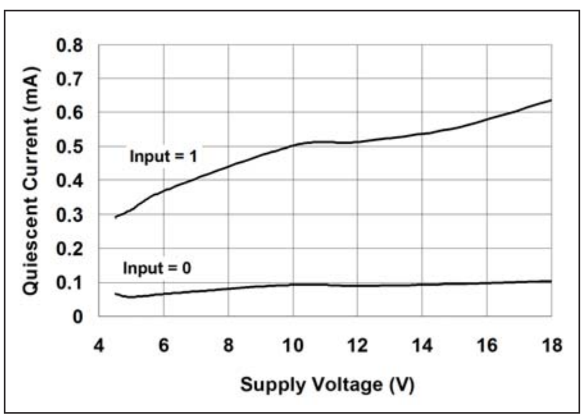


FIGURE 2-9: *Quiescent Current vs. Supply Voltage.*

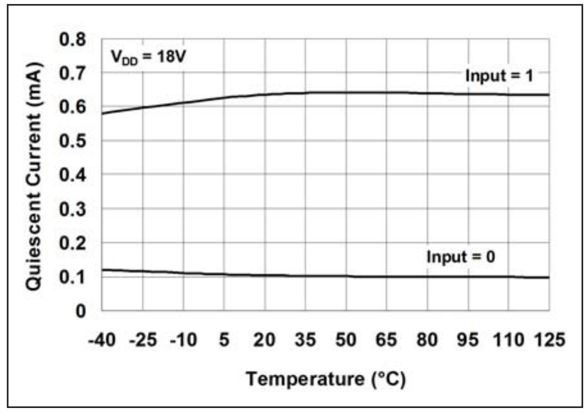


FIGURE 2-10: *Quiescent Current vs. Temperature.*

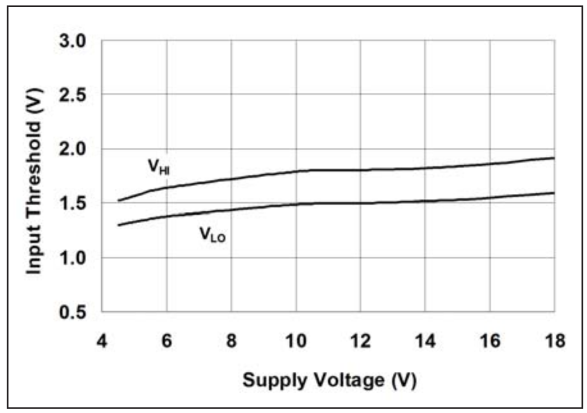


FIGURE 2-11: *Input Threshold vs. Supply Voltage.*

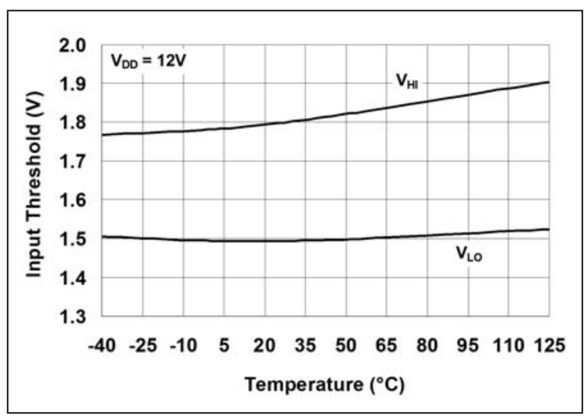


FIGURE 2-12: *Input Threshold vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ = 18V.

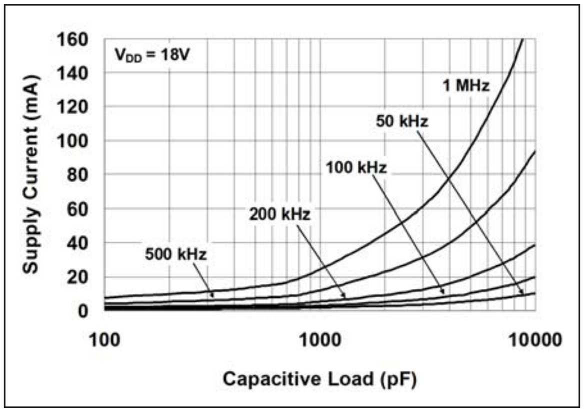


FIGURE 2-13: Supply Current vs. Capacitive Load.

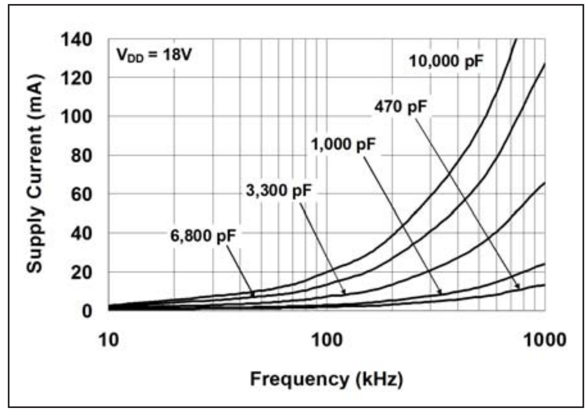


FIGURE 2-16: Supply Current vs. Frequency.

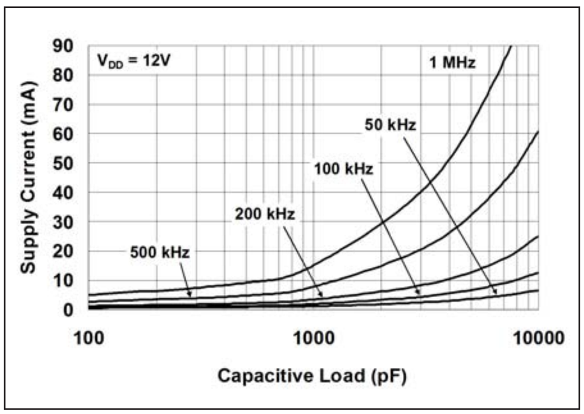


FIGURE 2-14: Supply Current vs. Capacitive Load.

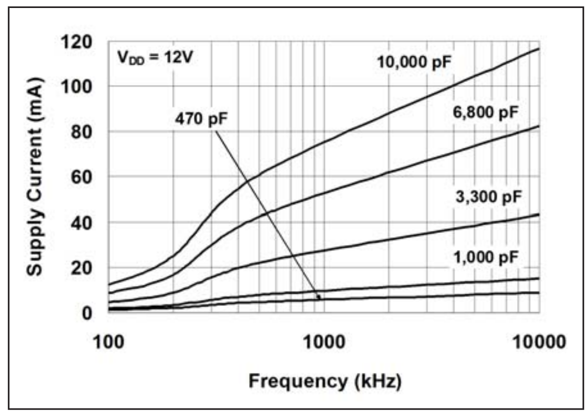


FIGURE 2-17: Supply Current vs. Frequency.

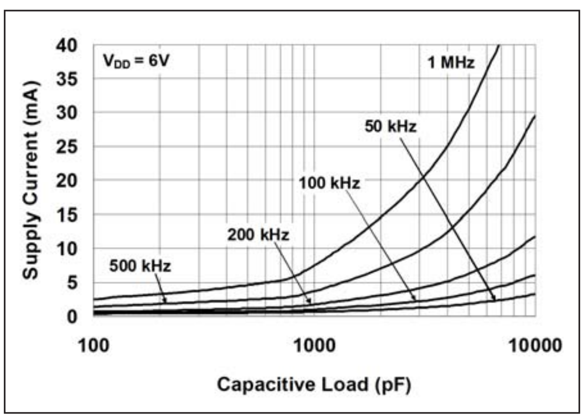


FIGURE 2-15: Supply Current vs. Capacitive Load.

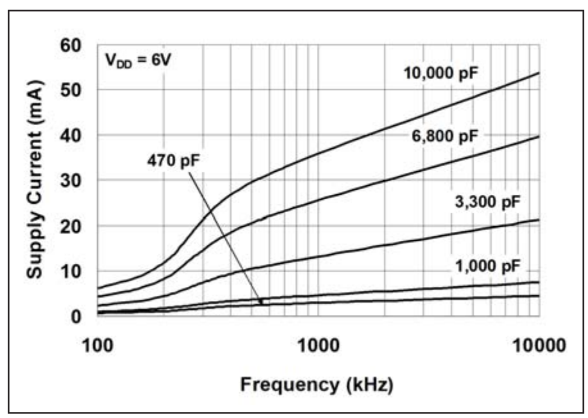


FIGURE 2-18: Supply Current vs. Frequency.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ = 18V.

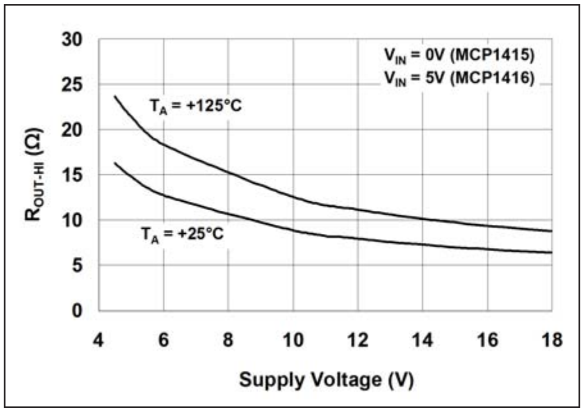


FIGURE 2-19: *Output Resistance (Output High) vs. Supply Voltage.*

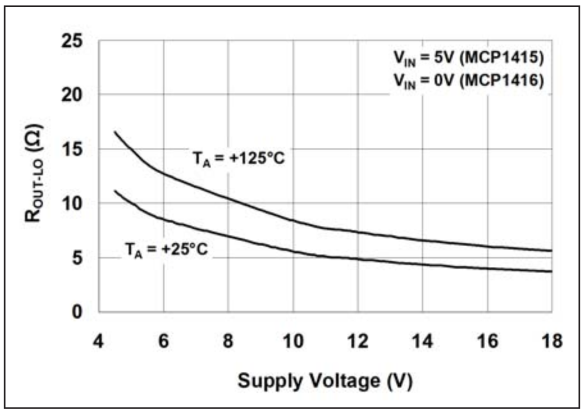


FIGURE 2-20: *Output Resistance (Output Low) vs. Supply Voltage.*

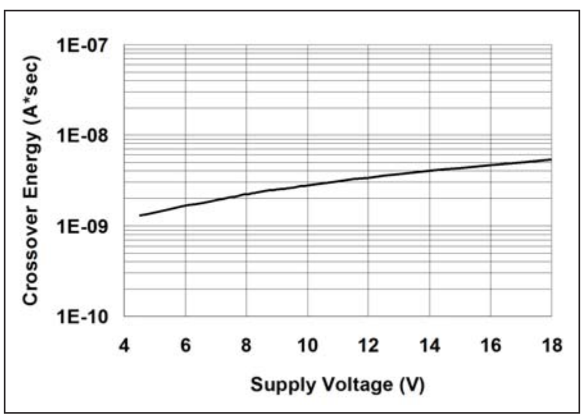


FIGURE 2-21: *Crossover Energy vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.		Symbol	Description
MCP1415/16	MCP1415R/16R		
1	1	NC	No Connection
2	5	V_{DD}	Supply Input
3	3	IN	Control Input
4	2	GND	Ground
5	4	$\overline{OUT}$/OUT	Output

3.1 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.2 Control Input (IN)

The MOSFET driver input is a high-impedance, TTL/CMOS compatible input. The input also has hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

3.3 Ground (GND)

Ground is the device return pin. The ground pin should have a low-impedance connection to the bias supply source return. When the capacitive load is being discharged, high peak currents will flow out of the ground pin.

3.4 Output (OUT, $\overline{OUT}$)

The output is a CMOS push-pull output that is capable of sourcing and sinking 1.5A of peak current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET stays in the intended state even during large transients. This output also has a reverse current latch-up rating of 500 mA.

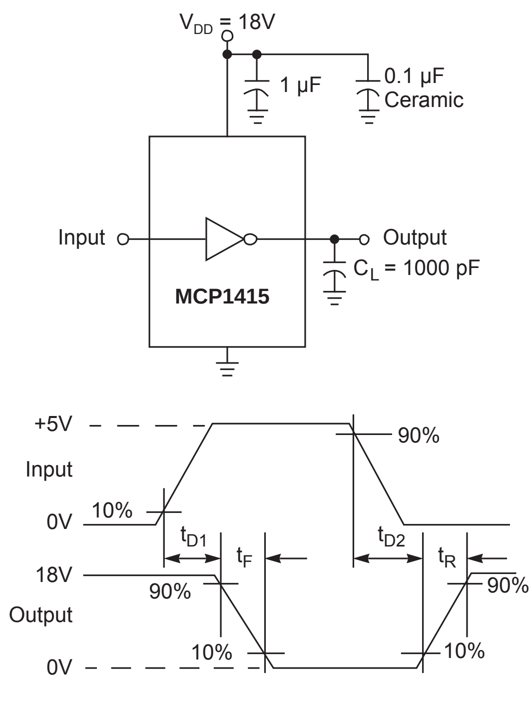
4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high peak currents to charge/discharge the gate capacitance of external MOSFETs or Insulated-Gate Bipolar Transistors (IGBTs). In high frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver such as the MCP1415/16 family can be used to provide additional source/sink current capability.

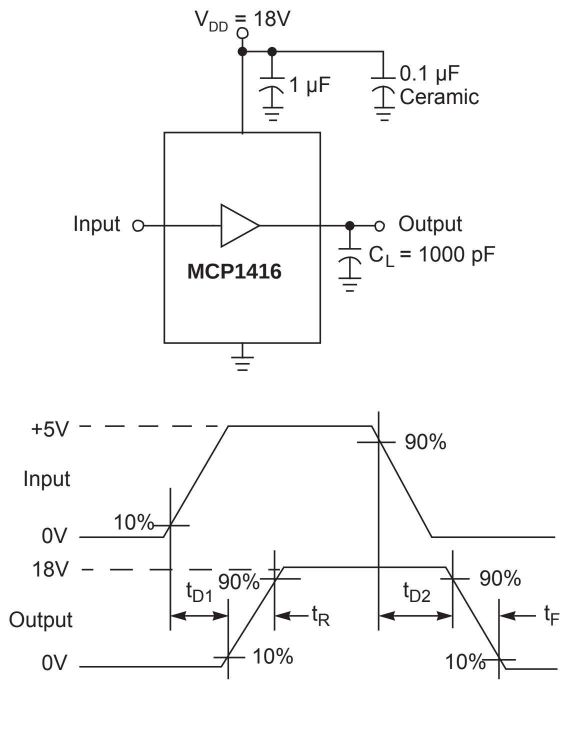
4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state is characterized by the driver's rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP1415/16 timing.



Note: Input Signal: $t_{RISE} = t_{FALL} \le 10$ ns
100 Hz, 0-5V Square Wave

FIGURE 4-1: Inverting Driver Timing Waveform.



Note: Input Signal: $t_{RISE} = t_{FALL} \le 10$ ns
100 Hz, 0-5V Square Wave

FIGURE 4-2: Non-Inverting Driver Timing Waveform.

4.3 Decoupling Capacitors

Careful layout and decoupling capacitors are required when using power MOSFET drivers. Large current is required to charge and discharge capacitive loads quickly. For example, approximately 720 mA are needed to charge a 1000 pF load with 18V in 25 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place a ceramic and a low ESR film capacitor in parallel between the driver V_{DD} and GND. A 1.0 µF low ESR film capacitor and a 0.1 µF ceramic capacitor placed between pins 2 and 4 are required for reliable operation. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.4 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

P_T	=	Total power dissipation
P_L	=	Load power dissipation
P_Q	=	Quiescent power dissipation
P_{CC}	=	Operating power dissipation

4.4.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of the frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in Equation 4-2.

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

f	=	Switching frequency
C_T	=	Total load capacitance
V_{DD}	=	MOSFET driver supply voltage

4.4.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends on the state of the input pin. The MCP1415/16 devices have a quiescent current draw of 0.65 mA (typical) when the input is high and of 0.1 mA (typical) when the input is low. The quiescent power dissipation is shown in Equation 4-3.

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

I_{QH}	=	Quiescent current in the High state
D	=	Duty cycle
I_{QL}	=	Quiescent current in the Low state
V_{DD}	=	MOSFET driver supply voltage

4.4.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because, for a very short period of time, both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation described in Equation 4-4.

EQUATION 4-4:

$$P_{CC} = CC \times f \times V_{DD}$$

Where:

CC	=	Cross-Conduction constant (A*sec)
f	=	Switching frequency
V_{DD}	=	MOSFET driver supply voltage

4.5 PCB Layout Considerations

Proper PCB layout is important in high-current, fast switching circuits to provide proper device operation and robustness of design. Improper component placement may cause errant switching, excessive voltage ringing or circuit latch-up. PCB trace loop area and inductance must be minimized. This is accomplished by placing the MOSFET driver directly at the load and placing the bypass capacitor directly at the MOSFET driver (see Figure 4-3). Locating ground planes or ground return traces directly beneath the driver output signal reduces trace inductance. A ground plane also helps as a radiated noise shield and it provides some heat sinking for power dissipated within the device (see Figure 4-4).

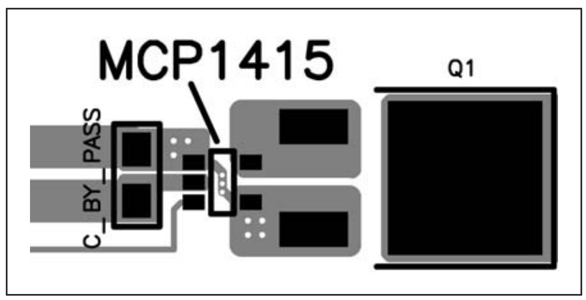


FIGURE 4-3: Recommended PCB Layout (TOP).

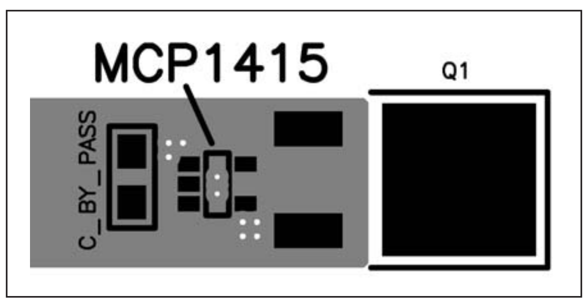
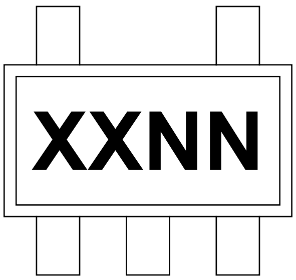


FIGURE 4-4: Recommended PCB Layout (BOTTOM).

5.0 PACKAGING INFORMATION

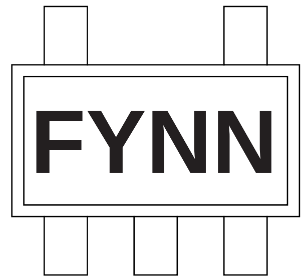
5.1 Package Marking Information

5-Lead SOT-23



Standard Markings for SOT-23	
Part Number	**Code**
MCP1415T-E/OT	FYNN
MCP1415RT-E/OT	F7NN
MCP1416T-E/OT	FZNN
MCP1416RT-E/OT	F8NN

Example



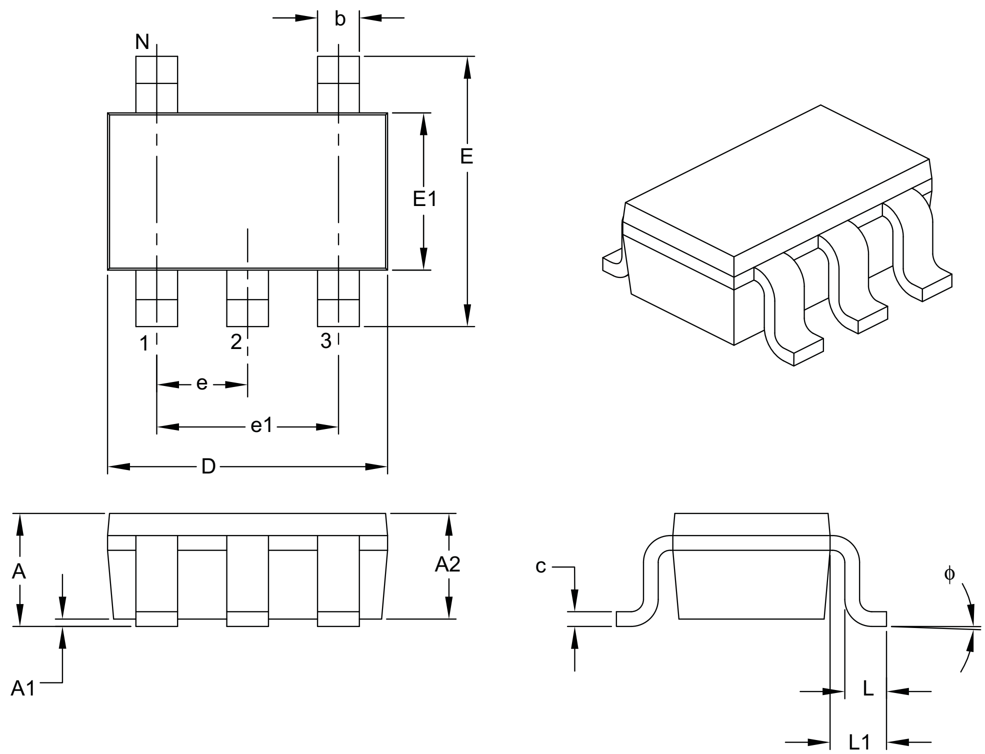
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

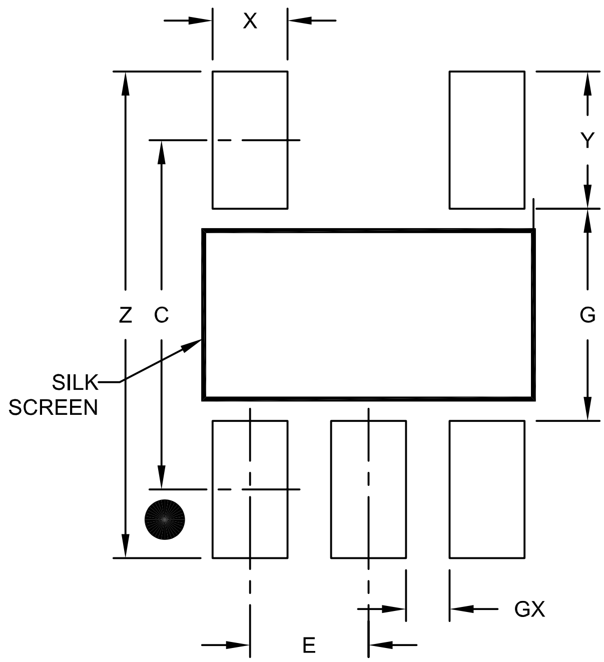
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

APPENDIX A: REVISION HISTORY

Revision G (June 2016)

The following is the list of modifications:

1. Updated Features.
2. Updated **Section "DC Characteristics"**.
3. Updated **Section "DC Characteristics (Over Operating Temperature Range) (Note 1)"**.
4. Updated Figure 2-3, Figure 2-6, Figure 2-7 and Figure 2-8.
5. Updated Figure 4-1 and Figure 4-2.
6. Minor typographical corrections.

Revision F (July 2014)

The following is the list of modifications:

1. Fixed a typographical error for the electrostatic discharge (ESD) value in Absolute Maximum Ratings †.
2. Minor grammatical and editorial corrections.

Revision E (May 2012)

The following is the list of modifications:

1. Updated the Electrostatic Discharge (ESD) value.

Revision D (December 2010)

The following is the list of modifications:

1. Updated Figure 2-19 and Figure 2-20.
2. Updated the package outline drawings.

Revision C (December 2008)

The following is the list of modifications:

Added the MCP1415R/16R devices throughout the document.

Revision B (June 2008)

The following is the list of modifications:

1. **Section "DC Characteristics"**, Switching Time, Rise Time: changed from 13 to 20.
2. **Section "DC Characteristics"**, Switching Time, Fall Time: changed from 13 to 20.
3. **Section "DC Characteristics (Over Operating Temperature Range) (Note 1)"** (Over Operating Temperature Range), Switching Time, Rise Time: changed maximum from 35 to 40.
4. **Section "DC Characteristics (Over Operating Temperature Range) (Note 1)"** (Over Operating Temperature Range), Switching Time, Rise Time: changed typical from 25 to 30.
5. **Section "DC Characteristics (Over Operating Temperature Range) (Note 1)"** (Over Operating Temperature Range), Switching Time, Fall Time: changed maximum from 35 to 40.
6. **Section "DC Characteristics (Over Operating Temperature Range) (Note 1)"** (Over Operating Temperature Range), Switching Time, Fall Time: changed typical from 25 to 30.

Revision A (June 2008)

Original release of this document.

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